AMENDMENTS TO THE CLAIMS

1. (Original) A programmable logic device, comprising:

a configurable logic block, the configurable logic block having function generators, each of the function generators configurable for at least two programmable mode functions;

the function generators coupled to an array of memory cells, the array of memory cells for storing configuration bits for configuring the function generators;

a primary address line coupled to each memory cell of the array of memory cells in a segment spanning two or more of the function generators;

a secondary address line coupled to groups of memory cells of the array of memory cells in separate segments, each of the separate segments spanning only one function generator of the function generators, the groups of memory cells being respectively associated with the function generators; and

a mask circuit configured to selectively communicate a signal of the primary address line to a segment of the secondary address line or to a ground responsive in part to the programmable mode function programmed.

2. (Original) The programmable logic device, according to claim 1, wherein the mask circuit is configured to selectively communicate the signal in partial response to operation state of the configurable logic block.

3. (Original) The programmable logic device, according to claim 2, wherein the operation state is a read state.

4. (Original) The programmable logic device, according to claim 2, wherein the operation state is a write state.

5. (Original) The programmable logic device, according to claim 2, wherein the at least two programmable mode functions are a lookup table and a random access memory.

6. (Original) The programmable logic device, according to claim 2, wherein the at least two programmable mode functions are a lookup table and a shift register.

7. (Original) The programmable logic device, according to claim 1, wherein the groups of memory cells are sub-arrays of the array of memory cells.

8. (Original) The programmable logic device, according to claim 7, wherein the sub-arrays have a row width of sixteen.

9. (Original) The programmable logic device, according to claim 7, wherein the sub-arrays have a column width of one.

10. (Original) The programmable logic device, according to claim 1, wherein a portion of memory cells of the array of memory cells is not part of the groups of memory cells respectively associated with the function generators.

11. (Original) The programmable logic device, according to claim 10, wherein each of the memory cells in the portion of memory cells is spaced apart for segmentation of the secondary address line.

12. (Original) The programmable logic device, according to claim 11, wherein each of the memory cells in the portion of memory cells is not usable.

13. (Original) The programmable logic device, according to claim 11, wherein the array of memory cells is eighty rows by one column.

14. (Original) The programmable logic device, according to claim 13, wherein the portion of memory cells are located at positions <16>, <22>, <39>, <56>, <62> and <79> of the array of memory cells.

Claims 15-26. (Cancelled)

27. The method, according to claim 25, wherein the static and continuous masking comprises grounding address lines of the portion of the memory cells in partial response to a masking signal.